Please amend the application as follows:

In the Claims

Please add new Claims 11-18.

11. (New) A method as claimed in Claim 6 wherein the phase of the edge of the input signal is directly compared with the phase of the edge of the output signal in combinational circuitry having an output which depends only on the state of its input.

12. (New) A method as claimed in Claim 6 wherein the phase comparator produces up and down pulses which, when the phase of the edge of the input signal is aligned with the phase of the edge of the output signal, are each a fraction of the input signal and the output signal transition times.

13. (New) A method as claimed in Claim 6 wherein the phase of the edge of the input signal is directly compared with the phase of the edge of the output signal by applying the input signal and output signal to gates of transistors which are coupled in a combinational logic circuit.

14. (New) A method as claimed in Claim 13 wherein the combinational logic circuit provides current source and drain to an output as up and down current pulses.

15. (New) A method as claimed in Claim 1 wherein the phase of the edge of the input signal is directly compared with the phase of the edge of the output signal in combinational circuitry having an output which depends only on the state of its input.

16. (New) A method as claimed in Claim 1 wherein the phase comparator produces up and down pulses which, when the phase of the edge of the input signal is aligned with the